2826

Attorney Docket SEL 174

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of)
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Yamazaki et al.)
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Serial No.: 09/544,801)
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Filed: April 7, 2000)
)
For: Semiconductor Device And)
Method For Fabricating The Same)
)
Art Unit: 2826)
)
Examiner: F. Erdem)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents , P.O. Box 1450, Alexandria, VA 22313-1450 on

December 11, 2003
(Date of Deposit)
Shannon Wallace
Name of applicant, assignee, or Registered Rep.
Shannon Wallace 12/11/03
Signature Date

Commissioner for Patents
P. O. Box 1450
Alexandra, VA 22313-1450

RESPONSE (B)

Sir:

Applicants have the following response to the Office Action of September 11, 2003.

In the Office Action, the Examiner has the following rejections under 35 USC §103(a):

A. Claims 1, 3, 4, 6, 8 and 9 are rejected under 35 USC §103(a) as being unpatentable over Yamanaka et al. '215 in view of Kobayashi et al. '930 further in view of Yamazaki et al ' 858.

B. Claims 10, 12, 13, 15, 17, 18, 19, 21, 22, 24, 26 and 27 are rejected under 35 USC §103(a) as being unpatentable over Yamanaka et al. '215, in view of Kobayashi et al. '930 in further in view of Yamazaki et al. '858.

C. Claims 64, 66, 67, 68, 70, 71, 72, 74, 75, 76, 78 and 79 are rejected under 35 USC §103(a) as being unpatentable over Seo '068 in view of Kobayashi et al. '930 further in view of Yamazaki et al '858.

D. Claims 65 and 69 are rejected under 35 USC §103(a) as being unpatentable over Seo '068 in view of Kobayashi et al. '903 in view of Iwanaga et al. '692 further in view of Yamazaki et al. '858.

E. Claims 73 and 77 are rejected under 35 USC §103(a) as being unpatentable over Seo in view of Kobayashi et al. further in view of Sasano et al. further in view of Yamazaki et al.

Each of these rejections is respectfully traversed.

The present invention is directed to a semiconductor device, and in particular, a semiconductor device having structural features such as those shown in Figs. 6A-6C (top view) or in Figs. 8A-8C (cross-sectional view) of the present application. Independent Claims 1, 10, and 19 of the present application are directed to a semiconductor device and recite that the gate electrode (e.g. 128 and 129 in the drawings) and the gate wiring (e.g. 147) are electrically connected with each other at a portion outside the channel-forming region. Independent Claims 64, 68, 72 and 76 of the present application are also directed to a semiconductor device and recite that the gate wiring is provided outside the channel region. Further, all of the independent claims at issue in this application recite that the gate electrode comprises a first conductive layer and the gate wiring comprises a second conductive layer.

In the Office Action, the Examiner admits that Yamanaka, Kobayyashi, Seo, Iwanaga and Sasano fail to disclose the required connection structure outside the channel forming region, as recited in the rejected claims. The Examiner, however, contends that Yamazaki "disclose a semiconductor device and fabrication method thereof where the required connection structure is disclosed."

Applicants cannot find the required structure in Yamazaki, and the Examiner has not pointed out where this structure is allegedly shown in Yamazaki. Accordingly, Applicants respectfully submit that the rejections under 35 USC §103(a) of the claimed invention over the cited references is improper. Therefore, it is requested that these rejections be withdrawn.

Conclusion

It is respectfully submitted that the present application is in a condition for allowance and should be allowed.

If any fee should be due for this amendment, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date: December 11, 2003

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